REMARKS

Claims 2-22 will be pending upon entry of the present amendment. Claims 2-6, 10, 16, and 17 have been amended, and claim 1 is canceled. New claims 19-22 are herein submitted.

Claims 4 and 5 have been amended to depend from claim 2. Claims 16 and 17 are each amended to correct minor grammatical errors. These amendments have not been made for reasons of patentability, nor do they change the scope of the respective claims. Claims 2 and 3 have been placed in independent form, and have been amended to incorporate the limitations of claim 1.

The Examiner has rejected claim 2 under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly define the subject matter which the applicants regard as their invention. In particular, the Examiner finds the line, "loading using the external matrix cell array" unclear. Accordingly, the word "loading" has been deleted from claim 2, which now recites, "using the external matrix cell array to simulate the matrix array of memory cells of the semiconductor device." With this amendment, claim 2 is now allowable under Section 112, second paragraph.

The Examiner has objected to claims 1-3, 6, and 10 under 37 C.F.R. § 1.75. The Examiner has described particular concerns with respect to the above listed claims. In response to the objection, the listed claims have been amended as follows: the typo of claim 1 (now incorporated into claims 2 and 3) has been corrected to read "matrix"; claims 2 and 3 have each been amended to recite "testing the memory device"(claim 1 originally recited "testing the semiconductor device"); claim 6 has been reformatted to separate the limitation of the claim from the preamble; and claim 10 has been amended to read "the test control device," which further clarifies the scope of the limitation. These amendments concern matters of form, only, and do not affect the scopes of the respective claims.

Claims 1-5, 6-8, and 16-18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Mullarkey et al. (U.S. Patent No. 5,732,033, hereafter "Mullarkey") in view of Bond et al. (U.S. Patent No. 4,450,559, hereafter "Bond"), further in view of Russ et al. (IEEE Reference, hereafter "Russ"). Claim 10 has been rejected under 35 U.S.C. § 103(a) as being

unpatentable over Mullarkey in view of Russ, and claims 8-15 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Mullarkey in view of Russ, and further in view of Kumakura et al. (U.S. Patent No. 5,566,386, hereafter "Kumakura").

Claims 2 and 3 have each been amended to include all the limitations of claim 1, and are now presented in independent form. Claim 1 has been canceled.

Claim 2 recites the limitations of

> loading test data and/or instructions into the control logic circuit portion using a test operation control device, temporarily, said test operation control device being external of, and temporarily connected to, said memory device, said test operation control device having a matrix cell array external to the memory device; and
>
> testing the memory device by using the external matrix cell array to simulate the matrix array of memory cells of the semiconductor device.

In rejecting claim 2, the Examiner states,

> Mullarkey teaches to use "an integrated memory device 10" (see Figure 1) comprising "a memory array 12", including "a plurality of memory cells 22", "control circuit 16", and "a test mode 20" provided for operating the memory device 10 in a test regime.

The Examiner proceeds to acknowledge that Mullarkey does not explicitly point out the use of two memories, relying on Bond for this teaching, and further acknowledges that Mullarkey and Bond in combination fail to teach an external test operation, relying, in turn, on Russ for this teaching.

With respect, the applicants disagree with the Examiner's position. The cited combination of references fails to teach or suggest all the limitations of claim 2.

Not only does Mullarkey not teach two memories, it also fails to teach an external test operation control device, and further fails to teach or suggest using an external matrix cell array to simulate the matrix array of memory cells of the semiconductor device.

In citing the Bond reference, the Examiner states that Bond teaches two memories, and further states

> It is well known that most integrated circuits do not contain the test operation memory.... Accordingly, it would have been obvious...to modify Mullarkey with the teaching of Bond by simply using one memory as internal and a second memory as external.

However, Bond fails to provide any suggestion or motive to support such a position. In particular, Bond is directed to a memory system that includes surplus memory as replacement cells for faulty memory cells. Bond states,

> The portion of Figure 4 within the dotted box 29 is one of thirty-six identical alternate data storage sections also referred to as replacement units.... The selection control block 36 functions generally to address locations in the alternate memory units 31 and 32 to replace the effective bit cells in the main memory 30.

(Column 3, lines 34-51).

A review of Bond, including the above cited text, reveals that the separate memory provided by Bond is for the purpose of replacing defective memory, and thus is not available for testing purposes. See, also, for example, column 2, lines 9-13, which read,

> It is, therefore, an object of the present invention to provide a memory system for storing data in which a minimum amount of auxiliary storage is required to store data that cannot be stored in defective locations of the main memory.

Accordingly, Bond fails to teach or suggest a test operation control device having a matrix cell array external to the memory device, as recited in claim 2. With respect to the actual testing operation, Bond is completely silent as to how such an operation is carried out, providing only the assumption that such an operation can be performed. In describing the operation of its inventive method, Bond states the following,

> Assume that a diagnostic check was made of each of the word addresses in main memory and that at each word address, each of the defective cells was identified.... Stated differently, it will be assumed that word addresses between 0 and 256K may contain some defective cell positions, but that addresses above 256K contain no defects. The following discussion will, therefore, be limited to treatment of identified faults....

Clearly, Bond provides no teaching with respect to the methods or devices used for the purpose of testing a memory array, and so, fails to teach "using the external matrix cell array to simulate the matrix array of memory cells of the semiconductor device," as recited by claim 2.

Additionally, Bond fails to teach "a test operation control device...temporarily connected to said memory device," as recited by claim 2. The "secondary memory unit 13" of Bond, cited by the Examiner as providing this teaching, is clearly a permanent part of the data

processing system of Bond's Figure 1 (see, for example, column 2, lines 56-59), and so cannot be regarded as being temporarily connected.

Even if Bond were capable of providing the missing teachings of claim 2, it would be inappropriate to combine Bond with Mullarkey.

MPEP § 2143.01 states:

> If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the reference are not sufficient to render the claims *prima facie* obvious.

The Examiner has indicated that "it would have been obvious...to modify Mullarkey with the teaching of Bond by simply using one memory as internal and a second memory as external."

Applicants understand the Examiner to mean that it would have been obvious to replace the spare rows of memory provided internally by Mullarkey (column 3, lines 61-63) with external memory, as provided by Bond. However, these spare rows are fundamental to the proper function of the Mullarkey invention (column 4, lines 61-64, column 9, lines 19-29), which is directed to a device having onboard circuitry for self-test during fabrication (column 3, lines 42-47). Accordingly, a modification such as that suggested by the Examiner would, at the least, change the principle of operation of Mullarkey. Thus, such a combination is inappropriate.

Bond is not analogous art, as compared to the device to which claim 2 is directed, and is thus inappropriate as a prior art reference. The Examiner has stated that Bond "does not explicitly point out that both of [the] memories are internal, inherently teaching for any combinations (internal/external) of two memories." Applicants respectfully suggest that this statement is inapposite. Bond teaches a memory system having a plurality of memory chips, coupled via various busses to selection circuitry and other control circuitry residing on separate chips. See, for example, Figure 1, which shows the basic architecture of Bond's system, and Figure 1A, which shows the main memory 11, consisting of 144 columns of 64K chips (see also Figures 4 and 5, and column 3, lines 18-51 and column 4, lines 33-66). Bond's main memory, alone, includes more than 9,000 memory chips. Thus, Bond teaches that, not only are all 9,000 memories external with respect to each other, so also are all other functions, including control logic circuits.

To the extent that Bond teaches any testing at all—being directed to memory distribution after a test has been performed—, it is directed to testing data processing systems having control logic and memory spread across multiple substrates, and probably multiple circuit boards. Thus, methods, systems, or circuits, employed in the testing of a device such as that taught by Bond are not relevant or comparable to methods or systems used for testing a device that includes a control logic circuit, a matrix array of memory cells, and storage circuitry, integrated together on a semiconductor substrate, such as that recited in claim 2. Accordingly, combination of Bond with any reference for the purpose of teaching or suggesting such methods is inappropriate.

Referring now to the Russ reference, the Examiner has stated that it would have been obvious to modify the procedure of Mullarkey and Bond by including the external test operation as taught by Russ. This argument is moot however, inasmuch as the test operation taught by Russ is not analogous to the testing of claim 2, which recites,

> testing the memory device by using the external matrix cell array to simulate the matrix array of memory cells of the semiconductor device.

Russ does not teach using an external matrix cell array to simulate the matrix array of memory cells of the semiconductor device, as recited by claim 2. The only simulations taught by Russ are those used to evaluate the effectiveness of Russ's own testing configurations, and are not directed to the testing of particular devices (see paragraphs B and C of the second column of page 483). Russ is silent with respect to the testing of a memory device, or with using a memory array of the testing device to simulate the memory array of the device under test. In fact, it appears that Russ's tests are directed, for the most part, to detecting faults in high speed data path circuitry, and to testing general sequential circuits (see first paragraph, column 2, page 482). Russ fails to teach testing a memory device, and in particular, fails to teach or suggest testing a semiconductor memory device by using an external matrix cell array to simulate the matrix array of memory cells of the semiconductor device. This limitation is also neither taught nor suggested by either Mullarkey or Bond.

Even if Russ were sufficient to provide teachings that Mullarkey and Bond fail to teach, Russ teaches away from a combination with Mullarkey. Russ states that

> Built in self test techniques which are non-intrusive to the circuitry under test are investigated for incorporation in field programmable gate arrays and multi-chip modules.... These approaches incur no area or performance penalties yet diagnostic resolution can be obtained to the device level.

(See Russ's Abstract).

Russ also states,

> These BIST techniques are non-intrusive in that they do not require modifications to the internal portions of device under test and, therefore, do no incur the usual area and performance penalties.

(Column 2, second complete paragraph).

From the above, it is clear that Russ teaches toward a system in which all testing circuitry is provided external to the semiconductor devices to be tested. In contrast, Mullarkey teaches a system in which testing circuitry is provided on the semiconductor substrate for the purposes of self testing (see column 3, lines 42-47). A combination of the testing methods of Russ, as suggested by the Examiner, with the device of Mullarkey would render the testing circuitry of Mullarkey inoperative and change Mullarkey's principle of operation. Accordingly, such a combination is inappropriate for providing a *prima facia* case of obviousness (see MPEP § 2143.01).

Applicants stress that, while it is not unreasonable to assume that a device configured to test another electronic device may be expected to have a memory of its own, the mere existence of such a device does not in any way suggest that the memory might be used as a substitute for the memory array of a device under test, during the testing procedure. After all, the memory of a test device may be expected to be used to store test instructions, input data, or results, without necessarily or obviously being used as a substitute of another memory array.

In summary, claim 2 is allowable for at least the following reasons:

- Mullarkey, Bond, and Russ, each fail to teach a test operation control device having a matrix cell array external to the memory device, and using the external matrix cell array to simulate the matrix array of memory cells of the semiconductor device.
- Mullarkey is inadequate as a reference for combination with any other reference in teaching or suggesting the limitations of claim 2, inasmuch as Mullarkey teaches the formation of

test circuitry on board the device, and so teaches away from the limitations of claim 2, which recites the use of an external matrix cell array to test the semiconductor device.

- Bond cannot correct the deficiencies of Mullarky, since Bond offers no teachings as to methods of testing, but only to methods of response to a testing, and further, provides no teaching or suggestion as to the structure or operation of a test operation control device.
- Bond fails to teach a test operation control device having a memory array and temporarily connected to the memory device, teaching, instead, permanently connected backup memory.
- Bond is inappropriate as a reference for combination with any other reference in teaching or suggesting the limitations of claim 2, being instead directed to a system made up a large plurality of substrates, each performing a single function, and to providing replacement memory for faulty cells, and so differs radically from the structure to which the method of claim 2 is directed.
- Russ cannot provide the missing teaching, since Russ offers no teaching that remotely suggests employing an external matrix cell array to simulate an array of the device under test.
- Russ offers no teachings directed to the testing of a memory device, being directed instead to the testing of testing methods.
- To the extent that the actual test methods of Russ are discussed, they are not suggested as being appropriate for memory devices, but are apparently more directed to detecting faults in high speed data path circuitry, and to testing general sequential circuits.
- A combination of Russ with Mullarkey is inappropriate, since the teachings of Russ are in opposition, Mullarkey being directed to testing circuitry on the substrate, while Russ is directed to methods calculated to obviate the need for onboard testing circuitry, such that a combination would render Mullarkey's test circuits inoperative.

For at least these reasons, claim 2 is allowable over the cited prior art. Dependent claims 4 and 5 are also therefore allowable.

Claim 3 recites, in part,

> said test operation control device having a control logic external to the memory device; and

> testing the memory device by simulating the control logic circuit of the semiconductor device using the external control logic.

Claim 3 varies in scope from claim 2. In particular, claim 3 is directed to a method of testing the memory device by simulating the control logic circuit, while claim 2 is directed to simulating the memory array matrix. Nevertheless, it will be recognized that the arguments presented in support of the allowability of claim 2 may also be applied in support of the allowability of claim 3. It may be noted, in particular, that none of the references cited teach simulating the control logic circuit of the semiconductor device using an external control logic. Accordingly, claim 3 is allowable over the cited prior art.

Applicants have previously noted that none of the cited references teach or suggest "a memory unit external of and detachably connectable to the memory device, the memory unit configured to operate in substitution of the memory cell array during testing." as recited in claim 6. Accordingly, claim 6, together with claims 7 and 8, is allowable over the cited prior art.

Claim 16 recites,

> bypass circuitry formed on the substrate, and configured to permit substitution of an external memory array for the purpose of testing the control logic circuit separately from the memory array formed on the substrate.

Many of the arguments previously presented in support of claims 2, 3, and 6 may also be applied in support of claim 16. Accordingly, these arguments will not be repeated. While claim 16 varies significantly in scope from previously argued claims, the cited references nevertheless fail to teach or suggest the limitations of claim 16 for reasons that are clear, given a reading of the previously presented arguments. With reference to the above quoted limitation of claim 16, applicants note that, while Mullarkey does provide pass circuits (see column 4, line 63), Mullarkey's pass circuits are configured merely to provide fast equalization while the circuit device is being operated in its self-test mode (see column 6, lines 6-9), and cannot be considered bypass circuitry configured to permit substitution of an external memory array, as recited in claim 16. Such circuitry is neither taught nor suggested by any of the other cited art. For at least these reasons, claim 16, together with dependent claims 17 and 18, is allowable over the cited prior art.

In rejecting claim 9, the Examiner cites Kumakura as providing the missing teachings of Mullarkey stating, "Mullarkey does not explicitly teach and point out the external test control (device)...." The Examiner continues, stating that "Kumakura teaches the test control means including 'operation logic circuit 3', 'command register 2' (column 6, lines 61, 62), 'test cell 19', 'switching circuit 7' (column 6, line 64)...and other analogous means presented in the applicant's claims."

Applicants respectfully traverse this position. Applicants call the Examiner's attention to the paragraph of column 6 where the features cited by the Examiner are listed. Kumakura states, starting at line 55, that the associated Figure 2 "is a block diagram showing the configuration of a prior art flash memory." Kumakura proceeds, then, to list the features of that prior art flash memory, including the features cited by the Examiner as being part of the test control means. There is no test device mentioned or described. Nowhere in the document does Kumakura provide any teaching with respect to the structure of an external testing device. Accordingly, Kumakura fails to teach or suggest the limitation admitted by the Examiner as being missing from Mullarkey, namely a test control device.

Furthermore, as previously demonstrated, Mullarkey is directed to a device having extensive circuitry formed thereon for the purpose of self testing, and thus teaches away from an external test control device having a circuit for simulating the internal memory array to permit testing of the control logic circuit in isolation from the internal memory array, as recited in claim 9. Accordingly, Mullarkey cannot support a *prima facia* case of obviousness over claim 9.

Interestingly, Kumakura suffers from the same shortcoming. Kumakura, also, is directed to a device having extensive testing circuitry formed thereon. Kumakura incorporates a plurality of dummy cells and a corresponding test dummy cell signal input (see Figures 4-6 and column 8, lines 11-19 and 45-52). Kumakura teaches a device that includes additional test circuitry for the purpose of testing the operational circuitry of the device. Accordingly, Kumakura also teaches away from an external test control device as recited in claim 9.

In rejecting claim 9, the Examiner argues that it is well known that some integrated circuits do not contain the test control device. Such a statement may, or may not be true, but is not relevant to the question of the allowability of claim 9. Claim 9 is not limited to

devices that have or do not have test control circuitry. Demonstrating that a reference teaches away from the limitations of the claim because it teaches onboard testing circuits is not the equivalent of arguing that the claim in question does not read on integrated circuits containing test control devices, nor is it equivalent to arguing that an integrated circuit not having a test control device is appropriate invalidating prior art.

Kumakura also teaches away from the limitations of claim 9 for another reason. The Examiner will recognize, upon comparing the Background section of the present application with Kumakura's description of the prior art, that the present application and Kumakura are both directed to solutions of a similar problem. For example, the present application states,

> As is well known, a prominent feature of electronic non-volatile memory devices, *e.g.*, last-generation flash memory devices, is that a control logic circuit portion is incorporated in them to form an integral part the device. The control logic is not of inconsiderable complexity and importance being, as it is, requisite for executing program and erase algorithms.

(Paragraph beginning at page 1, line 6).

Referring now to column 7, line 12, Kumakura states,

> The recent flash memory design incorporates automatic circuitry that allows the writing and erasure of flash memory cells to be accomplished just by entering simple control commands from the outside.

Kumakura continues by describing known methods of testing such a memory device, and at line 27 of column 7, Kumakura states

> Therefore, to verify whether the status register is functioning correctly, the operational logic circuit is actually made to perform various operations to produce various status conditions, and the status register is tested to see whether it reflects the status correctly.

Kumakura proceeds, then, to point out some of the shortcomings of this method, including,

> The procedure does not guarantee that the status register will function properly when a failure occurs in the memory cell matrix or the sense amplifier/write amplifier.

(Column 7, lines 53-57).

Kumakura then describes its inventive solution, beginning at line 61 of column 7, in which test dummy cells and test dummy cell select signal input circuits are provided, for performing onboard testing. Following a description of the testing circuitry and procedures, Kumakura states,

> Thus, the testing is performed in a comprehensive manner, including the entire write and erase circuitry, to check the performance of the entire circuit including the automatic circuit for both cell normal and failed states.

(Column 12, lines 15-19).

Returning, now, to the Background section of the present application, several known methods of testing a memory device are described, beginning at line 8 of page 2. One of the methods described incorporates the formation of circuitry dedicated to the testing of the device, including special memory cells loaded with predetermined data sequences, stating,

> ...the control logic incorporates a hardware portion specially for performing test operations.
>
> In response to forcing said data sequence, the control logic provides something of a 'reaction to stimulus', and a record of the data sequences and their responses, when compared with expected results provided by a simulation, will allow conformity of the circuit with the specifications to be verified and guaranteed.

(Page 2, line 28-page 3, line 2).

A comparison of the Background section of the present application with Kumakura reveals that the solution taught by Kumakura is strikingly similar to the previously known solutions described in the Background section. In regard to such solutions the present application states,

> A drawback with the above testing method is that complex gates must be included in the design of the control logic portion devoted to testing, which expands the area requirements of the device to a considerable extent.

(Page 2, lines 2-5), and

> Again, the overall area for occupation by the circuit must be expanded, merely to enable the testing operations to be performed.

(Page 3, lines 10 and 11).

Clearly, Kumakura is directed to testing solutions that are known to the applicants and considered inadequate. Further, the solutions provided in the various embodiments of the invention, including those upon which claim 9 reads, are not improvements on known methods, such as those proposed by Kumakura, which provide for additional circuitry onboard, but rather, provide solutions that are not envisioned by Kumakura, and which Kumakura teaches away from.

Section 2143.02 of the MPEP states the following,

> The prior art can be modified or combined to reject claims as *prima facia* obvious as long as there is a reasonable expectation of success. (emphasis added)

In describing memory devices that incorporate circuitry for writing and erasing of the memory cells, but do not incorporate extensive onboard test circuitry, Kumakura states,

> Once the automatic circuitry is activated, it is not possible to know the status of internal circuitry without reading out the status register.

(Column 7, lines 18-20).

Clearly, Kumakura offers no reasonable expectation of success, in testing devices for which testing circuitry is not provided onboard, and thus is insufficient to establish a *prima facia* case of obviousness under Section 103.

For at least the reasons outlined above, claim 9, together with dependent claims 10-13, is allowable over the cited prior art.

Claim 14 recites:

> A method for testing a memory array integrated, with a control logic circuit, onto a semiconductor substrate, comprising:
>
> simulating the control logic circuit, using an external connected circuit;
>
> performing test operations with the memory array and the external connected circuit; and
>
> observing interactions between the memory array and the external connected circuit.

In rejecting claim 14, the Examiner again cites features listed by Kumakura in column 6 and referring to Figure 2, stating that Kumakura teaches simulation, or test control means. Applicants again point out that the referenced features are actually components of a prior

art circuit, and make no reference to testing procedures of any kind, let alone the simulation of the control logic circuit. The Examiner continues, acknowledging that

> Kumakura does not explicitly teach and point out the external location of any or some means, inherently teaching the use of a control circuit, a test mode and appropriate memory array (inherently internal)...for operating the memory device in a test regime.

Applicants note that this is precisely the test operation described in the Background of the present application, namely, a device having an internally formed test circuit for testing the device. However, the Examiner then proceeds to a conclusion, with which the applicants firmly disagree, stating,

> It would have been obvious...to modify Kumakura with the teaching of using the external location of any means for memory test, because it is obvious and well known, that the procedure for most tests and particularly for memory test control apparatus includes steps of simulating the circuits, performing the test, and observing interactions and results, considering the purpose of the testing equipment.

Applicants disagree with this position for at least three reasons: First, Kumakura considers and rejects external testing, and so teaches away from such a modification. MPEP § 2143.01 states:

> The mere fact that references <u>can</u> be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of the combination. (emphasis in original)

Accordingly, a modification of Kumakura as suggested by the Examiner is not obvious.

Second, Kumakura fails to teach or suggest simulating a control logic circuit, using an external connected circuit, or performing test operations with a memory array integrated, with the control logic circuit, onto a semiconductor substrate. Note that Kumakura is directed to testing the <u>status register and write/erase circuitry</u>, <u>not</u> the memory array, as recited in claim 14 (see, for example, column 7, lines 56-60, column 11, lines 33-36, and column 12, lines 15-19).

Third, the examiner's assertion that the steps of claim 14 are "obvious and well known" (i.e., common knowledge) is incorrect. Claim 14 is directed to the testing of a memory

array integrated with a control logic circuit. Most test methods for testing memories are not relevant to the question at hand, inasmuch as most memories are not integrated with control logic circuits on the same semiconductor device. Note, for example, the Bond reference cited by the Examiner in rejecting other claims of the present application, which employs more than 9,000 memory array substrates, none of which incorporates an onboard control logic circuit, but is instead controlled externally. The architecture of such memory devices is radically different from that of a device such as that to which claim 14 is directed, and so, methods of testing such devices are not comparable or analogous.

The only prior art reference cited in the current Office Action that provides any teaching directed to the testing of a memory device having an array integrated with a control logic circuit, is Kumakura. Kumakura teaches at least six separate methods of testing such a device (see, for example, column 2, lines 10-33, lines 45-64, line 65-column 3, line 8, column 3, lines 9-28, lines 29-46, column 7, lines 21-55, and column 11, line 33-column 12, line 19). None of the testing methods described by Kumakura entails using an external connected circuit to simulate the control logic circuit, as recited in claim 14. One would assume that if such methods were well known, Kumakura would have listed them among the known methods.

The evidence present in the cited references suggests that, at least in the case of memory devices such as that of claim 14, testing of such a device according to the steps of the method of claim 14 is not obvious or well known.

The MPEP § 2144.03(A) states,

> It is never appropriate to rely solely on 'common knowledge' in the art without evidentiary support in the record, as the principle evidence upon which a rejection is based.

The MPEP further states, in the same section, at letter (C),

> If applicant challenges a factual assertion as not properly officially noticed or not properly based upon common knowledge, the Examiner must support the finding with adequate evidence.

Accordingly, the applicants respectfully request that the Examiner provide a reference or references directed to memory devices having a memory array and a control logic

circuit integrated thereon, and teaching all the limitations of claim 14, without reference to what is practiced with reference to other types of memory devices.

It has previously been demonstrated that a combination of Russ with Mullarkey is inappropriate, inasmuch as Mullarkey teaches a need for the formation, on a semiconductor memory device, of onboard testing circuitry (see, for example, column 2, lines 8-15, lines 34-36, lines 44-48, etc.), while Russ teaches systems and methods for testing semiconductor devices without additional onboard circuitry, and further teaches away from the formation of onboard testing circuitry (see, for example, Russ's Abstract on page 480, the first two sentences of the second complete paragraph of the second column of page 480, final two sentences of the first column of page 485, etc.). Applicants now observe that Kumakura, which was also cited in combination with Mullarkey and Russ in rejecting claim 14, also teaches away from a combination with Russ, providing, as it does, additional test dummy cells and test dummy cell select signal input circuits (see, for example, column 8, lines 13-52), and further teaching the advantages of onboard testing circuitry. Accordingly, there is no motivation in either Mullarkey or Kumakura to combine Russ therewith, nor is there any motivation in Russ to combine with either Mullarkey or Kumakura. Additionally, a combination of Russ with either Mullarkey or Kumakura would change the principle of operation of the respective device. For at least these reasons a combination of Russ with Mullarkey or Kumakura is inappropriate.

While the scope of claim 15 differs from that of claim 14, many of the arguments and observations provided in support of the allowability of claim 14 may also be applied in support of the allowability of claim 15. Accordingly, those arguments will not be repeated here.

New claims 19-22 are directed to various embodiments of the invention, and are fully supported in the specification. While the scopes of these claims differ from those of previously presented claims, allowability of these claims will be obvious, given a reading of the previously presented arguments.

The Examiner has rejected the dependent claims of the present application under various combinations of the prior art references previously discussed. Inasmuch as the dependent claims each depend from a respective allowable base claim, the rejections of those claims are

moot, and so will not be further addressed here. Furthermore, the inadequacies of the cited references, both individually and in combination, has been well demonstrated.

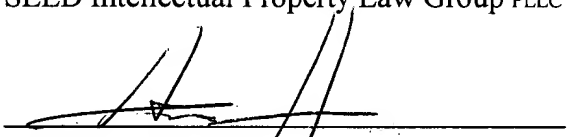
However, it should also be noted that many of these dependent claims are allowable on their own merits, apart from their allowability as depending from a base claim. The basis of those merits will be clear given a review of the comments and arguments presented with respect to the cited references, and so will not be further discussed.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative at (206) 622-4900 in order to expeditiously resolve prosecution of this application.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



Harold H. Bennett II
Registration No. 52,404

HHB:wt

Enclosure:
Postcard

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

856063.689 / 488440_1.DOC